UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/346,834	11/30/94	BOWLES	J 069400032C

EXAMINER	
~~RAY, G~~	

ART UNIT	PAPER NUMBER
2305	19

B3M1/0628

JENKENS & GILCHRIST, P.C.
1445 ROSS AVENUE
SUITE 3200
DALLAS, TX 75202-2799

DATE MAILED: 06/28/95

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), 0 days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____.

Part II SUMMARY OF ACTION

1. ☒ Claims 1, 3-11, 23-25 and 27-32 are pending in the application.

Of the above, claims _____ are withdrawn from consideration.

2. ☒ Claims 2, 12-18 and 26 have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 1, 3-11, 23-25 and 27-32 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

1. The examiner acknowledges the cancellation of claims 2, 12-18, 26 and addition of claims 27-32 by the amendment filed on Nov. 11, 1994.

2. Claims 1, 3-11, 23-25 and 27-32 are presented for examination.

3. Claims 1, 3-11, 23-25 and 27-32 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The examiner notes the following ambiguities.

As per claim 1, the preamble recites an apparatus for disabling a masked interrupt. However, the body of the claim recites unmasking the masked interrupt, i.e., enabling the interrupt. Clarification is required.

As per claims 3-11, the claims incorporate the deficiencies of the parent claim.

As per claim 23, the phrase "[in] a processor that may enter a predetermined state" (lines 1-2) is vague and indefinite because it is unclear as to what causes the processor to enter the predetermined state. What is the predetermined state? How many states are there? Clarification is required.

As per claims 24-25, the claims incorporate the deficiencies of the parent claim.

As per claim 27, the phrase "means for asserting said interrupt when said interrupt request is asserted ..." is vague and indefinite because it is unclear as to where the interrupt is asserted.

As per claims 28-32, the claims incorporate the deficiencies of the parent claim.

4. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

5. Claims 1, 3-9, 27, 28, 30 and 31 are rejected under 35 U.S.C. § 103 as being unpatentable over US Patent 4,344,133 issued to Bruce, Jr. et al. in view of US Patent 4,420,806 issued to Johnson, Jr. et al.

As per claim 1, Bruce, Jr. et al. teach the claimed:

"means for indicating a software condition; means for indicating a hardware condition": Bruce's means for indicating a

software condition; means for indicating a hardware condition (see col. 1, lines 49-52).

The reference of Bruce, Jr. et al. fails to expressly teach the limitation of "means for unmasking said masked interrupt ...". However, the above feature is well known to one of ordinary skill in the art at the time the invention was made as evidenced by Johnson, Jr. et al. The reference of Johnson, Jr. et al. teaches the feature in Fig. 2, element 21. It would be obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Bruce, Jr. et al. to implement the above feature of Johnson, Jr. et al. because that would allow Bruce's system to selectively handle interrupts. Therefore, it would be obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Bruce, Jr. et al. using the above feature of Johnson, Jr. et al. to obtain the claimed invention.

As per claim 3, Bruce teaches the "means for enabling" and "means for asserting" in col. 8, lines 51-56 and Johnson teaches "means for enabling an unmasked circuit" in Fig. 2, element 21. It would be obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Bruce, Jr. et al. to implement the above feature of Johnson, Jr. et al. because that would allow Bruce's system to selectively handle interrupts. Therefore, it would be obvious to one of ordinary skill in the

art at the time the invention was made to modify the system of Bruce, Jr. et al. using the above feature of Johnson, Jr. et al. to obtain the claimed invention.

As per claim 4, Bruce teaches the "programmable register that outputs a software enable signal" in col. 1, lines 62-64.

As per claim 5, Bruce teaches the "means for indicating said hardware condition comprises at least one hardware circuit, and wherein each of said at least one hardware circuit outputs a hardware enable signal" in col. 2, lines 52-53.

As per claim 6, the reference of Bruce, Jr. et al. fails to expressly teach the limitation of "means for enabling said unmasking circuit comprises OR gate that receives at least one of an indicated software condition enable signal an indicated hardware condition enable signal...". However, the above feature is well known to one of ordinary skill in the ar at the time the invention was made as evidenced by Johnson, Jr. et al. The reference of Johnson, Jr. et al. teaches the feature in Fig. 3, element 55 which is functionally same as the claimed limitation. It would be obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Bruce, Jr. et al. to implement the above feature of Johnson, Jr. et al. because that would allow Bruce's system to selectively handle interrupts. Therefore, it would be obvious to one of ordinary skill in the art at the time the invention was made to modify the system of

Bruce, Jr. et al. using the above feature of Johnson, Jr. et al. to obtain the claimed invention.

As per claim 7, the claim is rejected for analogous reasons as discussed in the rejection of claim 6.

As per claims 8-9, the claims are rejected for the same reasons as discussed in the rejection of claim 6 with the exception of "wherein said at least one hardware circuit asserts said hardware enable signal when said processor is in a particular state" (claim 8), "wherein said particular state comprises an idle mode" (claim 9). However, it would be obvious choice of design because that would efficiently utilize processing time of any system such as applicant's. It is the continuing goal of a system designer to improve the system performance using up to date technology available in the art at the time the invention was made.

As per claim 27, the claim is rejected for analogous reasons as discussed in the rejection of claims 1 and 6 above.

As per claims 28, 30 and 31, the claims are rejected for the same reasons as discussed in the rejection of claims 7-9 respectively.

6. Claims 23-25 are rejected under 35 U.S.C. § 103 as being unpatentable over US Patent 5,249,284 issued to Kass et al. in view of US Patent 4,420,806 issued to Johnson, Jr. et al.

As per claim 23, Kass et al. teach the claimed:

"a first subcircuit that receives a first signal for indicating whether said processor is in said predetermined state ... produces an unmasking signal": Kass' first subcircuit that receives a first signal for indicating whether said processor is in said predetermined state ... produces an unmasking signal (see Fig 2A, output of element 50 and col. 4, lines 59-68);

"a second subcircuit that receives said unmasking signal ... produces a second interrupt signal": Kass' second subcircuit that receives said unmasking signal ... produces a second interrupt signal (see Fig 2A, output of element 46 and col. 4, lines 59-68); and

"a third subcircuit responsive to said interrupt signal for interrupting said processor": Kass' third subcircuit responsive to said interrupt signal for interrupting said processor (see Fig 2A, output of element 62 and col. 4, lines 59-68).

The reference of Kass et. al. fails to expressly teach the limitation of "a circuit for unmasking a masked interrupt". However, the above feature is well known to one of ordinary skill in the art at the time the invention was made as evidenced by Johnson, Jr. et al. The reference of Johnson, Jr. et al. teaches the feature in Fig. 2, element 21. It would be obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Kass et al. to implement the above feature of Johnson, Jr. et al. because that would allow Kass' system to

selectively handle interrupts. Therefore, it would be obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Kass et al. using the above feature of Johnson, Jr. et al. to obtain the claimed invention.

As per claim 24, the reference of Kass et al. shows "said predetermined state is an idle state" in Fig. 3, element 76.

As per claim 25, the reference of Kass et al. shows "said second subcircuit comprises an AND gate" in Fig. 2A, element 46.

7. Claims 10-11, 29 and 32 are objected to as being dependent upon a rejected base claim.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is urged to consider the references. However, the references should be evaluated by what they suggest to one versed in the art, rather than by their specific disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gopal C. Ray whose telephone number is (703) 305-9647.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Gopal C. Ray

GOPAL C. RAY
PRIMARY EXAMINER
GROUP 2300